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APPLICATION NO.	FII	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/372,879 08/12/1999		08/12/1999	STEFANOS SIDIROPOULOS	RD-036	1940
27846 .	7590	03/17/2003			
RAMBUS I			EXAMINER		
	1440 EL CAMINO REAL LOS ALTOS, CA 94022			FARAHANI, DANA	
				ART UNIT	PAPER NUMBER
				2814	
				DATE MAIL ED: 03/17/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	pplicant(s)
Advisory Action	09/372,879	SIDIROPOULOS ET AL.
nancery near	Examiner	Art Unit
<u> </u>	Dana Farahani	2814
The MAILING DATE of this communication appe	ars on the cover sheet with the c	correspondence address
THE REPLY FILED 03 March 2003 FAILS TO PLACE TI Therefore, further action by the applicant is required to av final rejection under 37 CFR 1.113 may <u>only</u> be either: (1) condition for allowance; (2) a timely filed Notice of Appeal Examination (RCE) in compliance with 37 CFR 1.114.	oid abandonment of this applica a timely filed amendment whicl	ation. A proper reply to a h places the application in
PERIOD FOR RE	PLY [check either a) or b)]	
a) The period for reply expires 3 months from the mailing date b) The period for reply expires on: (1) the mailing date of this A no event, however, will the statutory period for reply expire Is ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS 706.07(f). Extensions of time may be obtained under 37 CFR 1.136(a). The fee have been filed is the date for purposes of determining the period of fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of 1(2) as set forth in (b) above, if checked. Any reply received by the Officitimely filed, may reduce any earned patent term adjustment. See 37 C	Advisory Action, or (2) the date set forth ater than SIX MONTHS from the mailing FILED WITHIN TWO MONTHS OF THE date on which the petition under 37 CF of extension and the corresponding amount the shortened statutory period for reply the later than three months after the mail	g date of the final rejection. HE FINAL REJECTION. See MPEP R 1.136(a) and the appropriate extension unt of the fee. The appropriate extension originally set in the final Office action; or
1. A Notice of Appeal was filed on Appellant's 37 CFR 1.192(a), or any extension thereof (37 CFF		
2. The proposed amendment(s) will not be entered be	ecause:	
(a) they raise new issues that would require further	er consideration and/or search (s	see NOTE below);
(b) they raise the issue of new matter (see Note b	elow);	
(c) they are not deemed to place the application ir issues for appeal; and/or	n better form for appeal by mate	rially reducing or simplifying the
(d) they present additional claims without cancelling NOTE:	ng a corresponding number of fi	nally rejected claims.
3. Applicant's reply has overcome the following rejection	on(s):	
4. Newly proposed or amended claim(s) would canceling the non-allowable claim(s).	be allowable if submitted in a se	eparate, timely filed amendment
5. ☑ The a) ☐ affidavit, b) ☐ exhibit, or c) ☑ request for application in condition for allowance because: See		dered but does NOT place the
6. The affidavit or exhibit will NOT be considered becaraised by the Examiner in the final rejection.	ause it is not directed SOLELY to	o issues which were newly
7. For purposes of Appeal, the proposed amendments explanation of how the new or amended claims we		
The status of the claim(s) is (or will be) as follows:		
Claim(s) allowed:		
Claim(s) objected to:	,	
Claim(s) rejected: <u>1-24 and 26-37</u> .		()
Claim(s) withdrawn from consideration:	, / /	
8. The proposed drawing correction filed on is	/ / / / /	royed by the Examiner.
9. Note the attached Information Disclosure Statemen	it(s)(PTO-1449) Paper No(s)	Ta proced
10. Other:	SUPERVICORY TECHNOLO	PRIMARY TO THER JOY CENTER 2000
<u> </u>		
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Continuation of 5. does NOT place the application in condition for allowance because: in figure 14 of the Lee reference, 63 is the conductive pad, and 61 is underlying and surrounding the pad. Furthermore, while Lee is an ESD protection circuit and the Japanese patent a memory circuit, note that by applying the Japanese patent novelty to the ESD protection circuit of Lee, one of ordinary skill in the art could implement the device in Lee reference to a memory related application, while taking advantage of its ESD protection properties.